## REMARKS

Further to the Notice of Allowance mailed on May 16, 2008, in which the Examiner indicated that claims 1-8, 13-19 and 22-25 have been allowed, Applicants are submitting the present amendment, along with an RCE, in order to make changes to claim 1. Claims 1-8, 13-19 and 22-25 are all of the claims pending in the application.

Regarding claim 1, Applicants note that in the Office Action dated November 28, 2007, claim 1 was rejected under 35 U.S.C. §102(e) as being anticipated by Koizumi et al. (US 7,015,964).

By the present amendment, Applicants note that claim 1 has been amended so as to recite that the electric charge simultaneous removal unit includes timing generation circuits each having: a first switch transistor that serves as a switch;a capacitor disposed between a gate and a drain of the first switch transistor; and a second switch transistor connected to the gate of the first switch transistor, wherein charging the capacitor prevents a voltage drop in the reset signal applied from a source of the first switch transistor of one of the timing generation circuits and in the readout signal applied from a source of the first switch transistor of another one of the timing generation circuits, and wherein the reset signal is applied to a gate of the reset transistor, and the readout signal is applied to a gate of the readout transistor to simultaneously reach a high level and maintain the high level for a time period, the reset transistor and the readout transistor being included in each of the photoelectric conversion circuits disposed in the region to be read out.

Applicants respectfully submit that Koizumi does not disclose or suggest the above-noted features recited in amended claim 1.

In particular, regarding Koizumi, Applicants note that in Fig. 1 of this reference, a pixel of a solid-state image pickup device is depicted which includes a transfer switch Q1, a reset switch Q2, a transistor Q3 acting as an amplifier, and a selection switch Q4 (see col. 4, line 60 through col. 5, line 2). As explained in Koizumi with reference to the timing charts shown in Figs. 2 and 8, a diffusion region FD is reset to the reference voltage by inputting a high level pulse such as RST to the gate of the reset switch Q2, and a photoelectric converter PD is reset by inputting a high level pulse such as TX to the gate of the transfer switch Q1 (see col. 4, lines 26-27;col. 5, lines 30-32 and col. 7, lines 13-19).

Based on the foregoing description, Applicants note that while Koizumi discloses the ability to input a high level pulse RST to the reset switch Q2 and a high level pulse to the gate transfer switch Q1, that Koizumi does not teach, suggest or otherwise render obvious the features of an electric charge simultaneous removal unit that includes timing generation circuits each having: a first switch transistor that serves as a switch; a capacitor disposed between a gate and a drain of the first switch transistor; and a second switch transistor connected to the gate of the first switch transistor, wherein charging the capacitor prevents a voltage drop in the reset signal applied from a source of the first switch transistor of one of the timing generation circuits and in the readout signal applied from a source of the first switch transistor of another one of the timing generation circuits, and wherein the reset signal is applied to a gate of the reset transistor, and the readout signal is applied to a gate of the readout transistor to simultaneously reach a high level and maintain the high level for a time period, the reset transistor and the readout transistor being included in each of the photoelectric conversion circuits disposed in the region to be read out, as recited in amended

claim 1.

In view of the foregoing, Applicants submit that claim 1 is patentable over Koizumi, an indication of which is kindly requested.

Further, Applicants note that the remaining prior art applied in the Office Action of November 27, 2007 (i.e., Satoshi (JP 2000-078484) and the Applicant's Admitted Prior Art (AAPA)) does not cure the above-noted deficiencies of Koizumi.

For example, regarding Satoshi, Applicants note that this reference discloses the use of a solid state imaging device 3 having a mechanical shutter 2 arranged thereon (see Fig. 3 and Abstract). As explained in Satoshi, exposure of the imaging device is started by simultaneously resetting all of the pixels of the imaging device 3 in the state of opening the mechanical shutter 2 (see Abstract and paragraph [0011]). Regarding the AAPA, as shown in Fig. 3, a timing generation circuit includes a bootstrap circuit 146 that functions as a capacitor, and a transistor 148. As explained on page 3 of the specification, when electric charge is accumulated in the bootstrap circuit 146, a reset signal RSCELL is output to a reset transistor of each pixel.

Based on the foregoing, Applicants note that while (1) Satoshi discloses starting exposure by simultaneously resetting all of the pixels of the imaging device 3 in the state of opening the mechanical shutter 2, and (2) the AAPA discloses the use of a capacitor and a switch transistor 148 that enables a reset signal to be output to each pixel, that Satoshi and the AAPA do not teach, suggest or otherwise render obvious the features of an electric charge simultaneous removal unit that includes timing generation circuits each having: a first switch transistor that serves as a switch; a capacitor disposed between a gate and a drain of the first

switch transistor; and a second switch transistor connected to the gate of the first switch transistor, wherein charging the capacitor prevents a voltage drop in the reset signal applied from a source of the first switch transistor of one of the timing generation circuits and in the readout signal applied from a source of the first switch transistor of another one of the timing generation circuits, and wherein the reset signal is applied to a gate of the reset transistor, and the readout signal is applied to a gate of the readout transistor to simultaneously reach a high level and maintain the high level for a time period, the reset transistor and the readout transistor being included in each of the photoelectric conversion circuits disposed in the region to be read out, as recited in amended claim 1.

In view of the foregoing, Applicants respectfully submit that amended claim 1 is patentable over the cited prior art, an indication of which is kindly requested. Regarding claims 2-8, 24 and 25, Applicants note that these claims are patentable at least by virtue of their dependency on claim 1. Regarding claims 13-19, 22 and 23, Applicants note that no changes have been made to these claims, and therefore, that such claims remain patentable over the cited prior art.

In view of the above, Applicants respectfully submit that all of the claims of the present application are in condition for allowance.

If any points remain in issue which the Examiner feels may best be resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Shigetaka KASUGA et al.

/Kenneth W. Fields/
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By: _____
Kenneth W. Fields
Registration No. 52,430
Attorney for Applicants

KWF/krg
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250
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